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Customer No.: 31561
Docket No.: 11583-US-PA
Application No.: 10/708,209

AMENDMENTS

In The Claims

1-3. (cancelled)

4. (currently amended) A ~~design of a mask~~ for a thin film transistor (TFT) array substrate, wherein the mask has a display element area and a non-display element area, the mask comprising:

a plurality of pixel patterns disposed in ~~[[a]]the~~ display element area;

a plurality of peripheral circuit patterns disposed in ~~[[a]]the~~ non-display element area; and

a plurality of stitching pixel patterns disposed in a portion of the non-display element area adjacent to the display element area.

5. (currently amended) The ~~design of a mask~~ of claim 4, further comprising a plurality of driving element bonding patterns disposed at an edge of the display element area.

6. (currently amended) The ~~design of a mask~~ of claim 4, wherein the non-display element area is disposed at two edges of the display element area.

7. (currently amended) A thin film transistor (TFT) array substrate having a non-panel-display area and a panel-display area, comprising:

a plurality of pixel structures, disposed in a panel-display component;

a plurality of peripheral circuits, disposed in ~~[[a]]the~~ non-panel-display area; and

a plurality of stitching pixel structures, disposed in the non-panel-display area, wherein the

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stitching pixel structures and the pixel structures are connected in the non-panel-display area.

8. (original) The thin film transistor (TFT) array substrate of claim 7, further comprising a plurality of driving element bonding areas disposed at an edge of the panel-display area.

9. (original) The thin film transistor (TFT) array substrate of claim 7, wherein the non-display element area is disposed at two edges of the display element area.

10. (currently amended) A thin film transistor (TFT) array substrate having a non-panel-display area and a panel-display area, comprising:

a plurality of pixel structures, disposed in a panel-display component;

a plurality of first stitching pixel structures, disposed in the panel-display component, wherein the stitching pixel structures are adjacent to the pixel structures;

a plurality of peripheral circuits, disposed in ~~the~~ the non-panel-display area; and

a plurality of second stitching pixel structures, disposed in the non-panel-display area, wherein the first stitching pixel structures of the panel-display component and the second stitching pixel structures of the non-panel-display area are connected in the non-panel-display area.